CLAIMS

The invention claimed is:

1. A method of forming a plurality of capacitor devices, comprising:

forming conductive capacitor electrode material within openings in a first material comprising silicon and oxygen;

providing a retaining structure in physical contact with at least some of the conductive capacitor electrode material, the retaining structure comprising a dielectric material;

removing at least some of the first material while the retaining structure physically contacts the at least some of the conductive capacitor electrode material; and

after removing at least some of the first material, incorporating the conductive capacitor electrode material into a plurality of capacitor devices.

2. The method of claim 1 wherein the dielectric material of the retaining structure comprise silicon and nitrogen.

3. The method of claim 2 wherein the conductive capacitor electrode material is formed within the openings in the shape of upwardly-opening container structures.

4. The method of claim 2 wherein the conductive capacitor electrode material fills the openings to form conductive pedestals within the openings.

5. The method of claim 2 wherein the first material consists of one or more electrically insulative materials.

6. The method of claim 5 wherein the first material is over a semiconductor substrate, wherein the retaining structure is over the first material; and wherein the first material has a thickness of from about 5,000Å to about 50,000Å between the substrate and the retaining structure.

7. The method of claim 5 wherein the first material is over the retaining structure.

8. The method of claim 2 wherein the first material comprises one or more of borophosphosilicate glass, spin-on-glass, silicon dioxide, phosphosilicate glass, borosilicate glass, and silicon nitride.

9. The method of claim 2 wherein the retaining structure comprises silicon nitride.

10. The method of claim 9 wherein the silicon nitride has a thickness of from about 50Å to about 3000Å.

11. The method of claim 2 wherein the first material comprises borophosphosilicate glass and the retaining structure comprises silicon nitride.

12. The method of claim 2 wherein the first material comprises borophosphosilicate glass, wherein a wet etch is utilized to remove at least some of the first material; and wherein the retaining structure comprises silicon nitride and a material having increased selectivity to borophosphosilicate glass than silicon nitride during the wet etch.

13. The method of claim 12 wherein the material having increased selectivity to borophosphosilicate glass than silicon nitride during the wet etch consists essentially of silicon.

14. The method of claim 12 wherein the material having increased selectivity to borophosphosilicate glass than silicon nitride during the wet etch includes polycrystalline silicon.

15. The method of claim 14 wherein the polycrystalline silicon is over the silicon nitride.

16. The method of claim 15 wherein the polycrystalline silicon has a thickness of from about 50Å to about 1000Å.

17. The method of claim 15 wherein the polycrystalline silicon has a thickness of from about 50Å to about 1000Å; and wherein the silicon nitride has a thickness of from about 50Å to about 3000Å.

18. The method of claim 14 wherein the polycrystalline silicon is under the silicon nitride.

19. The method of claim 14 wherein the polycrystalline silicon is over and under the silicon nitride.

20. The method of claim 19 wherein the polycrystalline silicon below the silicon nitride has a thickness of from about 50Å to about 500Å; wherein the polycrystalline silicon above the silicon nitride has a thickness of from about 50Å to about 500Å; and wherein the silicon nitride has a thickness of from about 50Å to about 1000Å.

21. The method of claim 14 wherein the polycrystalline silicon entirely surrounds the silicon nitride.

22. A method of forming a plurality of capacitor devices, comprising:

providing a construction comprising a first material over a substrate;

forming a retaining structure over at least a portion of the first material;

forming openings extending into the first material;

forming conductive structures within the openings utilizing a first conductive layer, the conductive structures having outer sidewalls along the first material;

removing at least some of the first material to expose at least portions of the outer sidewalls of the conductive structures, the retaining structure retaining the conductive structures during the removal of the first material;

forming a capacitor dielectric material along the exposed portions of the outer sidewalls; and

forming a second conductive layer over the capacitor dielectric material.

23. The method of claim 22 wherein the retaining structure is formed before forming the openings, and wherein the openings extend through the retaining structure.

24. The method of claim 22 wherein the conductive structures are container structures having openings extending therein, and wherein the dielectric material and second conductive layer are formed to extend within the openings that extend into the container structures.

25. The method of claim 22 wherein the conductive structures are pedestals.

26. The method of claim 23 wherein the openings extend in an array comprising rows and columns; wherein the conductive structures are formed in the array defined by the openings and thus the conductive structures are within an array comprising rows and columns; and wherein the retaining structure is patterned to extend between and connect alternating pairs of the rows of the conductive structure array.

27. The method of claim 23 wherein the retaining structure is a second retaining structure; and wherein a first retaining structure is formed prior to forming at least some of the first material.

28. The method of claim 27 wherein a first portion of the first material is formed prior to forming the first retaining structure and a second portion of the first material is formed after forming the first retaining structure; and wherein the first retaining structure is patterned prior to forming the second portion of the first material so that some of the second portion of the first material is formed directly against the first retaining structure and some of the second portion of the first material is formed directly against the first portion of the first material.

29. The method of claim 23 wherein the retaining structure is a second retaining structure; wherein a first retaining structure is formed prior to forming the first material; and wherein the first material is between the first and second retaining structures.

30. The method of claim 22 wherein the retaining structure comprises silicon nitride.

31. The method of claim 22 wherein the first material comprises borophosphosilicate glass; wherein an isotropic etch is utilized to remove at least some of the first material, and wherein the retaining structure comprises silicon nitride and a material having increased selectivity to borophosphosilicate glass than silicon nitride during the isotropic etch.

32. The method of claim 31 wherein the material having increased selectivity to borophosphosilicate glass than silicon nitride during the isotropic etch consists essentially of silicon.

33. The method of claim 31 wherein the material having increased selectivity to borophosphosilicate glass than silicon nitride during the isotropic etch includes polycrystalline silicon.

34. The method of claim 33 wherein the polycrystalline silicon is over the silicon nitride.

35. The method of claim 33 wherein the polycrystalline silicon is under the silicon nitride.

36. The method of claim 33 wherein the polycrystalline silicon is over and under the silicon nitride.

37. The method of claim 33 wherein the polycrystalline silicon entirely surrounds the silicon nitride.

38. The method of claim 22 further comprising removing the retaining structure from over the first material after forming the second conductive layer.

39. A method of forming a plurality of capacitor devices, comprising:

providing a construction comprising a first material over a substrate;

forming openings extending into the first material; the openings extending in an array comprising rows and columns;

forming a first conductive layer within the openings, the first conductive layer within the openings forming container structures having outer sidewalls along the first material wherein the container structures are formed in the array defined by the openings and thus the container structures are within an array comprising rows and columns;

providing a retaining structure which extends between and connects alternating pairs of the rows of the container structure array, the retaining structure being directly against the first conductive layer of the container structures;

removing at least some of the first material to expose at least portions of the outer sidewalls of the container structures, the retaining structure retaining the container structures during the removal of the first material;

forming a capacitor dielectric material along the exposed portions of the outer sidewalls and within the container structures; and

forming a second conductive layer over the capacitor dielectric material.

40. The method of claim 39 wherein the retaining structure is beneath the first material.

41. The method of claim 39 wherein the retaining structure is over the first material.

42. The method of claim 41 wherein the retaining structure is a second retaining structure; and wherein a first retaining structure is beneath at least some of the first material.

43. The method of claim 39 wherein the first material comprises one or more of borophosphosilicate glass, spin-on-glass, silicon dioxide, phosphosilicate glass, borosilicate glass, and silicon nitride.

44. The method of claim 39 wherein the retaining structure comprises silicon nitride.

45. The method of claim 44 wherein the silicon nitride has a thickness of from about 50Å to about 3000Å.

46. The method of claim 39 wherein the first material comprises borophosphosilicate glass and the retaining structure comprises silicon nitride.

47. The method of claim 39 wherein the first material comprises borophosphosilicate glass, wherein a wet etch is utilized to remove at least some of the first material; and wherein the retaining structure comprises silicon nitride and a material having increased selectivity to borophosphosilicate glass than silicon nitride during the wet etch.

48. The method of claim 47 wherein the material having increased selectivity to borophosphosilicate glass than silicon nitride during the wet etch is a silicon-containing material.

49. The method of claim 48 wherein the silicon-containing material is over the silicon nitride.

50. The method of claim 49 wherein the silicon-containing material has a thickness of from about 50Å to about 1000Å.

51. The method of claim 49 wherein the silicon-containing material has a thickness of from about 50Å to about 1000Å; and wherein the silicon nitride has a thickness of from about 50Å to about 3000Å.

52. The method of claim 48 wherein the silicon-containing material is under the silicon nitride.

53. The method of claim 48 wherein the silicon-containing material is over and under the silicon nitride.

54. The method of claim 53 wherein the silicon-containing material below the silicon nitride has a thickness of from about 50Å to about 500Å; wherein the silicon-containing material above the silicon nitride has a thickness of from about 50Å to about 500Å; and wherein the silicon nitride has a thickness of from about 50Å to about 1000Å.

55. The method of claim 48 wherein the silicon-containing material entirely surrounds the silicon nitride.

56. A method of forming a plurality of capacitor devices, comprising:

providing a construction comprising a memory array region, a region other than the memory array region and a location between the memory array region and said other region;

forming a first material extending over the memory array region, over said other region, and over the location between the memory array region and said other region;

forming a second material over at least a portion of the first material that is over the memory array region and over an entirety of the first material that is over said other region;

forming openings extending into the first material over the memory array region and forming a trench within the first material over the location between the memory array region and said other region;

forming a first conductive layer within the openings and within the trench, the first conductive layer within the openings forming container structures having outer sidewalls along the first material;

after forming the first conductive layer and the second material, removing at least some of the first material to expose at least portions of the outer sidewalls of the container structures;

forming a capacitor dielectric material along the exposed portions of the outer sidewalls and within the container structures; and

forming a second conductive layer over the capacitor dielectric material.

57. The method of claim 56 wherein the second material comprises silicon nitride.

58. The method of claim 57 wherein the second conductive layer and the dielectric material are formed over the second material.

59. The method of claim 56 wherein the first material comprises borophosphosilicate glass; wherein an isotropic etch is utilized to remove the at least some of the first material; wherein the second material is incorporated into a retaining structure comprising the second material and a third material; wherein the second material comprises silicon nitride; and wherein the third material has increased selectivity to borophosphosilicate glass than does silicon nitride during the isotropic etch.

60. The method of claim 59 wherein the third material comprises one or both of amorphous silicon and polycrystalline silicon.

61. The method of claim 59 wherein the third material is over the silicon nitride.

62. The method of claim 59 wherein the third material is under the silicon nitride.

63. The method of claim 59 wherein the third material is over and under the silicon nitride.

64. The method of claim 56 wherein the first conductive layer comprises titanium nitride.

65. A semiconductor construction, comprising:

a substrate having a memory array region defined therein together with a region other than the memory array region and a location between the memory array region and said other region, said memory array region having a lateral periphery defined to entirely laterally surround the memory array region;

an electrically insulative material over said other region, the electrically insulative material having a lateral sidewall extending around the lateral periphery of the memory array region; and

an electrically conductive liner along the sidewall of the material; the electrically conductive liner laterally surrounding the lateral periphery of the memory array region.

66. The construction of claim 65 further comprising a silicon-nitride containing material over an entirety of said other region and in direct physical contact with the electrically conductive liner.

67. The construction of claim 65 wherein said electrically insulative material comprises BPSG, and wherein the silicon nitride-containing material is over the electrically insulative material.

68. The construction of claim 65 wherein the electrically conductive liner comprises titanium nitride.

69. The construction of claim 65 wherein the electrically conductive liner consists essentially of titanium nitride.

70. The construction of claim 65 wherein the electrically conductive liner consists of titanium nitride.

71. The construction of claim 65 wherein the electrically conductive liner is part of a trough; the trough having first sidewall corresponding to the electrically conductive liner and a second sidewall spaced from the first sidewall.

72. The construction of claim 71 wherein the second sidewall of the trough has an outer surface facing the memory array region and an inner surface facing the first sidewall; the construction further comprising a silicon nitride-containing layer directly against the outer surface of the second sidewall of the trough and extending toward the memory array region from the outer surface of the second sidewall of the trough.

73. The construction of claim 72 further comprising a plurality of capacitor constructions over the memory array region; the capacitor constructions extending in an array comprising rows and columns; the capacitor constructions comprising storage nodes which extend in the rows and columns of the array; and wherein the silicon nitride-containing layer extends between and connects alternating pairs of the rows of storage nodes of the array.

74. The construction of claim 65 further comprising a lateral periphery defined to entirely laterally surround said other region, and wherein the electrically conductive liner laterally surrounds the lateral periphery of said other region.

75. The construction of claim 74 wherein the electrically conductive liner comprises titanium nitride.

76. The construction of claim 74 wherein the electrically conductive liner consists essentially of titanium nitride.

77. The construction of claim 74 wherein the electrically conductive liner consists of titanium nitride.

78. The construction of claim 74 wherein the electrically conductive liner is part of a trough; the trough having first sidewall corresponding to the electrically conductive liner and a second sidewall spaced from the first sidewall.

79. A semiconductor construction, comprising:

a substrate having a memory array region defined therein together with a region other than the memory array region and a location between the memory array region and said other region;

a plurality of container structures across the memory array region; the container structures being electrically conductive and comprising inner sidewalls within the container structures and outer sidewalls in opposing relation to the inner sidewalls;

an electrically insulative material over said other region, the electrically insulative material having a lateral sidewall;

an electrically conductive liner along the sidewall of the material;

a capacitor dielectric material along the inner and outer sidewalls of the container structures; and

a second conductive layer over the capacitor dielectric material; the container structures, dielectric material and second conductive material together being incorporated into a plurality of capacitor constructions.

80. The construction of claim 79 wherein the memory array region has a lateral periphery defined to entirely laterally surround the memory array region; and wherein the electrically conductive liner laterally surrounds an entirety of the lateral periphery of the memory array region.

81. The construction of claim 79 further comprising a silicon-nitride containing material over an entirety of said other region and in direct physical contact with the electrically conductive liner.

82. The construction of claim 79 wherein said electrically insulative material comprises BPSG, and wherein the silicon nitride-containing material is over the electrically insulative material.

83. The construction of claim 79 wherein the electrically conductive liner and the capacitor containers comprise titanium nitride.

84. The construction of claim 79 wherein the electrically conductive liner comprises titanium nitride.

85. The construction of claim 79 wherein the electrically conductive liner consists essentially of titanium nitride.

86. The construction of claim 79 wherein the electrically conductive liner consists of titanium nitride.

87. The construction of claim 79 wherein the electrically conductive liner is part of a trough.

88. The construction of claim 87 wherein the trough has first sidewall corresponding to the electrically conductive liner and a second sidewall spaced from the first sidewall; the second sidewall having an outer surface facing the memory array region and an inner surface facing the first sidewall; the construction further comprising a silicon nitride-containing layer directly against the outer surface of the second sidewall of the trough and extending toward the memory array region from the outer surface of the second sidewall of the trough.

89. The construction of claim 88 wherein the container structures extend in an array comprising rows and columns; and wherein the silicon nitride-containing layer extends between and connects alternating pairs of the rows of the container structure array.

90. The construction of claim 88 further comprising at least one layer consisting essentially of silicon directly against the silicon nitride-containing layer.

91. The construction of claim 88 further comprising:

a first layer consisting essentially of silicon over and directly against the silicon nitride-containing layer; and

a second layer consisting essentially of silicon under and directly against the silicon nitride-containing layer.